

A Scalable Model Predictive Control with Integrated Power-Sharing Switching Function for Single-Phase N-Level Cascaded H-Bridge Inverters

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Abstract—This paper presents a scalable Model Predictive Control (MPC) strategy for single-phase N-level Cascaded H-Bridge (CHB) inverters, applicable to any odd number of voltage levels from $2k+1$ to 3^k . For the specific case of a 5-level inverter, an integrated power-sharing switching function with a simplified redundant-state management mechanism is introduced to ensure balanced power distribution among H-bridge modules and uniform switching losses. The study also analyzes the impact of load inductance estimation on MPC performance, showing how inductance selection influences current-tracking accuracy, switching behavior, and converter losses. The approach is validated through simulations and experiments on a SiC-based CHB inverter prototype operating in 5-, 7-, and 9-level configurations. Experimental results demonstrate precise current tracking, robust dynamic response, and, for the 5-level case, consistent power-sharing among modules, confirming the effectiveness and scalability of the proposed MPC for multilevel inverter applications.

Keywords: Balanced power-sharing, Cascaded H-Bridge inverter, Current tracking, Dynamic performance, Load inductance estimation, Redundant-state, Switching method.

I. INTRODUCTION

Multilevel inverters, particularly Cascaded H-Bridge (CHB) topologies, are increasingly employed in medium- and high-power grid-connected systems, motor drives, and renewable energy interfaces due to their modularity, fault tolerance, and ability to generate high-quality output waveforms with reduced filtering requirements [1]. In practical applications, CHB inverters (Fig. 1) often operate in asymmetric configurations, where DC sources have unequal voltages caused by battery aging, variations in solar irradiance, or differing fuel-cell characteristics. While asymmetry can reduce the number of modules required to achieve a given voltage level, it introduces significant control challenges, particularly as the number of levels increases [2, 3].

Conventional control strategies for CHB inverters typically combine proportional-integral (PI) current controllers

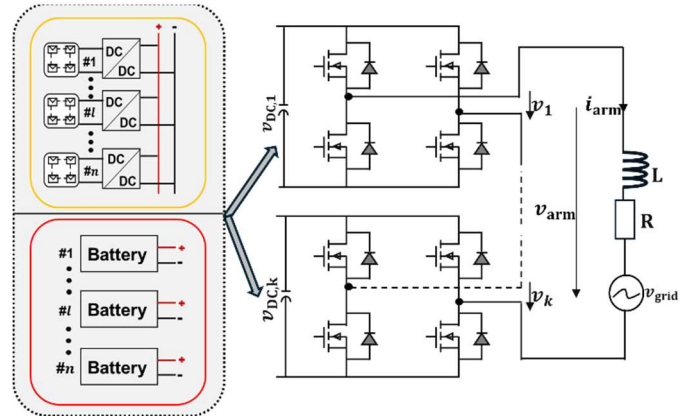


Fig. 1. CHB inverter configuration.

with carrier-based pulse-width modulation (PWM) [4], [5]. However, these approaches exhibit several limitations, including difficulty handling multivariable coupling, slow dynamic response, and the inability to explicitly enforce switching, current, or voltage constraints [6].

Model Predictive Control (MPC) offers significant advantages for CHB systems. MPC directly selects switching states, inherently handles constraints, and provides fast dynamic response without requiring a separate modulation stage [6], [7]. Despite these benefits, most existing MPC methods for single-phase CHB inverters lack the flexibility to manage redundant switching states, regulate module-level energy, or minimize device losses [8]. Moreover, conventional MPC suffers from exponential growth in switching combinations as the number of levels increases, limiting scalability [9]. Another critical limitation is the strong dependence of MPC on accurate knowledge of load parameters, particularly the load inductance; errors in inductance estimation can significantly affect current tracking, switching behavior, and overall converter losses [10]. Nevertheless, the sensitivity of MPC performance to inductance estimation errors remains insufficiently explored in the literature, especially in the context of high-level and asymmetric CHB inverters.

To address these challenges, this paper proposes a simplified and scalable MPC strategy for single-phase CHB inverters, capable of operating with any odd number of voltage levels. The method incorporates a power-sharing switching function specifically designed for a symmetrical two-cell CHB inverter, effectively managing redundant switching states to ensure balanced power among modules and uniform distribution of switching losses, without significantly increasing computational complexity. The proposed approach is validated through both PLECS-based simulations and experimental tests on 5-, 7-, and 9-level SiC-MOSFET CHB inverter prototypes. Results demonstrate the scalability of the control scheme, precise current tracking under varying operating conditions, and robust power-sharing performance for the 5-level case, confirming its suitability for high-performance and flexible multilevel inverter applications. Additionally, simulation results provide a systematic analysis of the impact of load inductance estimation on MPC performance, illustrating how inaccuracies influence current-tracking accuracy, switching behavior, and overall converter losses.

II. OPERATION OF SINGLE-PHASE SYMMETRICAL AND ASYMMETRICAL CHB INVERTERS

This section presents the generalized mathematical model of a single-phase CHB inverter composed of k isolated H-bridge cells, considering both symmetrical and asymmetrical DC-link configurations. Fig. 2(a) illustrates a single-phase two-cell CHB inverter. Each module is supplied by an isolated DC source $v_{DC,j}$ $j = 1, 2$ and can generate:

$$v_j(t) \in \{-v_{DC,j}, 0, v_{DC,j}\} \quad (1)$$

The output voltage of the inverter is the sum of the individual module voltages:

$$v_{arm}(t) = \sum_{j=1}^k v_j(t) \quad (2)$$

Defining the switching state of module j as $S_j(t) \in \{-1, 0, 1\}$

the module voltage can be expressed as:

$$v_j(t) = S_j(t)v_{DC,j} \quad (3)$$

and the total output voltage is given in Eq. (4). This equation is the fundamental voltage model from which symmetrical and asymmetrical cases derive. In the symmetrical configuration, all

DC sources have the same amplitude, $v_{DC,j} = v_{DC}$.

$$v_{arm}(t) = \sum_{j=1}^k S_j(t)v_{DC,j} \quad (4)$$

The total number of output voltage levels is:

$$N = 2k + 1 \quad (5)$$

Figure. 2(b) illustrates the switching states of a two-cell CHB inverter used to generate a 5-level output waveform.

In the asymmetrical configuration, the DC sources have different values. The total number of achievable voltage levels n (assuming all sums are distinct) is:

$$N = 2 \sum_{j=1}^k \frac{v_{DC,j}}{V_{step}} + 1 \quad (6)$$

where:

$$V_{step} = \min(v_{DC,1}, \dots, v_{DC,k})$$

is the smallest DC-link voltage, defining the unit voltage step. For instance, using $k = 2$ modules [Fig. 2(d)] with a geometric factor $r = 3$:

$$v_{DC,1} = 3V_{step} \text{ and } v_{DC,2} = V_{step}$$

Then the total number of levels:

$$N = 2 \frac{3V_{step} + V_{step}}{V_{step}} + 1 = 2(4) + 1 = 9$$

For asymmetrical CHB inverters, uniform multilevel output can still be achieved by carefully selecting the module voltages according to a geometric factor. For example, two asymmetric modules with a geometric factor of 2 produce a uniform 7-level output, as illustrated in Fig. 2(c), while the same modules with a geometric factor of 3 produce a uniform 9-level output, as illustrated in Fig. 2(d).

Figure. 3 compares the normalized arm voltage waveform for a CHB inverter composed of two H-bridge modules. In Fig. 3(a), the symmetric configuration ($v_{DC1} = v_{DC2}$) produces only five voltage levels, resulting in coarse voltage quantization and a relatively high total distortion harmonic $THD_{v_{arm}} = 27.02\%$. In contrast, Fig. 3(b) shows that selecting asymmetric DC sources based on a geometric factor increases the number of available voltage levels to nine and significantly reduces the $THD_{v_{arm}} = 13.88\%$. The finer quantization allows the

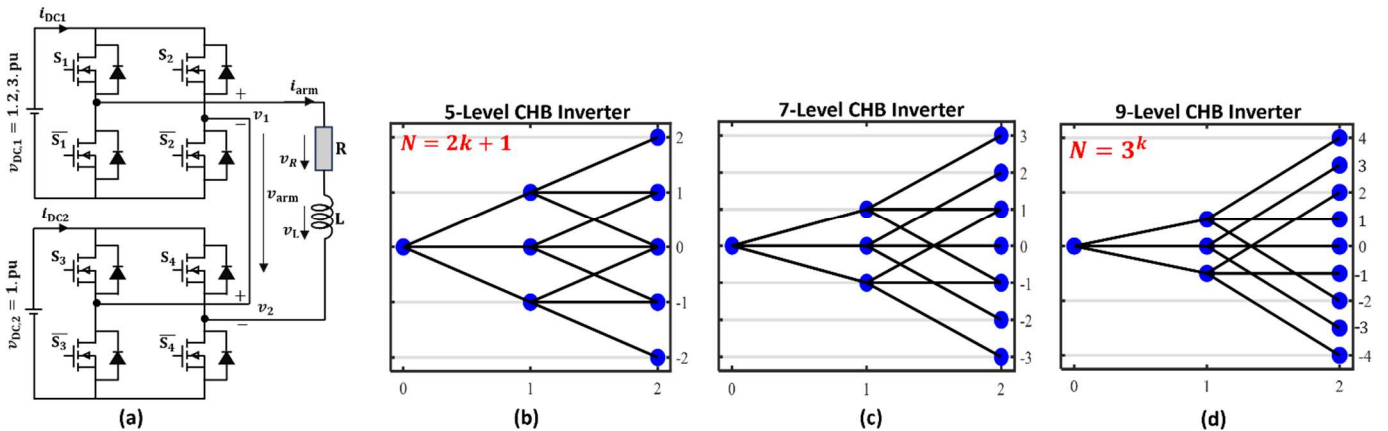


Fig. 2. (a) A two-cell CHB inverter with all its switching states to generate (b) 5-level voltage with $v_{DC1} = v_{DC2}$, (c) 7-level voltage $v_{DC1} = 2v_{DC2}$ and (d) 9-level voltage $v_{DC1} = 3v_{DC2}$.

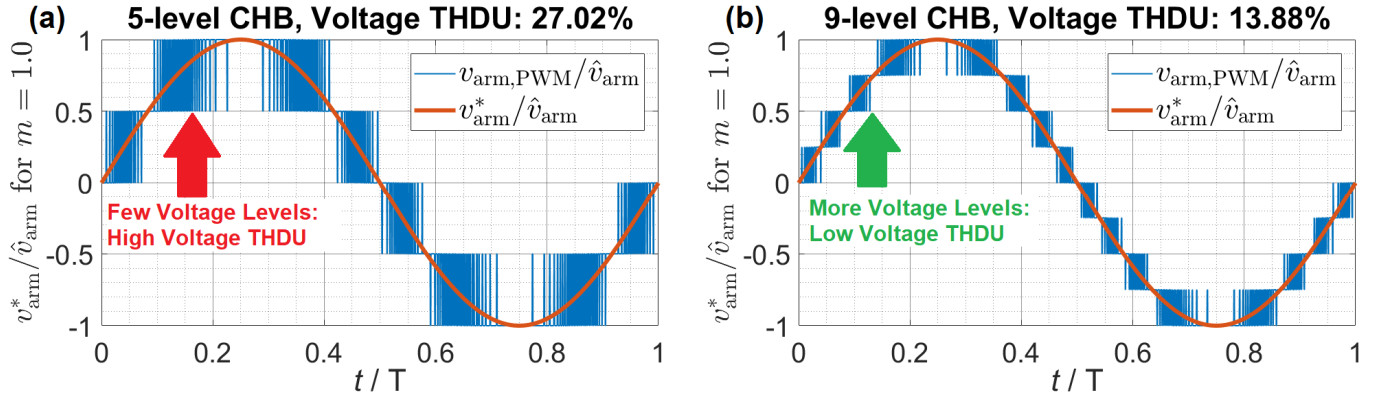


Fig. 3. (a) Comparison of 5-Level and 9-Level output voltage waveforms in a Two-Module CHB Inverter.

Mathematical model and discrete-time model of load current

- $v_{\text{arm}}(t) = Ri_{\text{arm}}(t) + L \frac{di_{\text{arm}}(t)}{dt}$
- $L \frac{di_{\text{arm}}(t)}{dt} = v_{\text{arm}}(t) - Ri_{\text{arm}}(t)$
- $\frac{di_{\text{arm}}}{dt} \approx \frac{i_{\text{arm}}[k+1] - i_{\text{arm}}[k]}{T_s}$

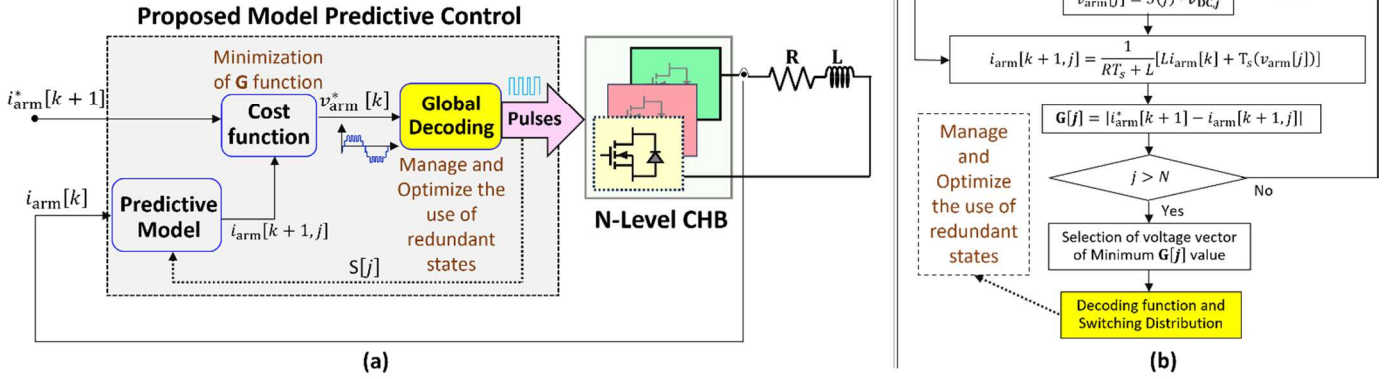


Fig. 4. (a) Block diagram of the proposed MPC scheme, (b) Flowchart of the proposed MPC.

synthesized voltage to more closely follow the sinusoidal reference. This comparison highlights the advantage of properly choosing asymmetric DC source values to increase the number of output levels without modifying the hardware.

III. PROPOSED MODEL PREDICTIVE CURRENT CONTROLLER FOR SINGLE-PHASE CHB INVERTERS

This section presents the theory and formulation of the proposed MPC scheme for single-phase CHB inverters. The approach targets current tracking accuracy, balanced power-sharing, and uniform switching losses across the inverter modules.

A. System Dynamics

Consider a single-phase CHB inverter connected to a RL load. The dynamics of the load-injected current $i_{\text{arm}}(t)$ are given by:

$$L \frac{di_{\text{arm}}(t)}{dt} = v_{\text{arm}}(t) - Ri_{\text{arm}}(t) \quad (7)$$

where:

L and R are the load inductance and resistance, $v_{\text{arm}}(t)$ is the instantaneous inverter output voltage.

For discrete-time implementation with sampling period T_s , Eq. (7) expressed as:

$$i_{\text{arm}}[k+1, j] = \left(1 - \frac{RT_s}{L}\right) i_{\text{arm}}[k] + \frac{T_s}{L} (v_{\text{arm}}[k]) \quad (8)$$

This linear prediction model enables forecasting the next current sample $i_{\text{arm}}[k+1]$ for different inverter switching states.

B. CHB Switching Model

For a CHB inverter with k H-bridge modules, each module voltage is:

$$v_j[k] = S_j[k] v_{\text{DC},j} ; S_j[k] \in \{-1, 0, 1\}$$

and the total inverter output voltage is:

$$v_{\text{arm}}[k] = \sum_{j=1}^k S_j[k] v_{\text{DC},j} \quad (9)$$

The set of feasible switching states $S[k] = [S_1[k], \dots, S_k[k]]^T$ determines all possible output voltages for the next sampling instant. Importantly, this formulation is general: it accounts for both symmetrical CHB inverters (all $v_{\text{DC},j}$ equal) and asymmetrical CHB inverters (different $v_{\text{DC},j}$) and can be applied

to any number of modules k , and thus to any number of output voltage levels N .

C. Predictive Control Principle

The MPC selects the optimal switching state by minimizing a cost function that quantifies the absolute difference between the predicted current and reference current:

$$G(S[k]) = \text{abs}(i_{\text{arm}}^*[k+1] - i_{\text{arm}}[k+1, j]) \quad (10)$$

The predicted current $i_{\text{arm}}[k+1, j]$ is obtained from (8) for each candidate switching vector $S[k]$. The optimal switching state minimizes the current error.

$$S_{\text{opt}}[k] = \arg \min_{S[k]} G(S[k]) \quad (11)$$

By directly using the individual module voltages $v_{\text{DC},j}$ in the prediction model and considering all feasible switching vectors, the MPC automatically accounts for asymmetrical DC sources and any number of output levels, providing consistent current tracking.

D. Control Algorithm

At each sampling period, T_s the controller performs:

- Measure the current $i_{\text{arm}}[k]$ and read the reference $i_{\text{arm}}^*[k+1]$.
- Predict future currents $i_{\text{arm}}[k+1, j]$ for all candidate switching states using (8).
- Evaluate the cost function (10).
- Select the optimal switching vector using (11)

The overall structure of the proposed MPC scheme is illustrated in Fig. 4(a), and its algorithmic flow is detailed in Fig. 4(b). In the proposed MPC algorithm, an aggregated voltage level command $v_{\text{arm}}^* \in \left\{ -\frac{(N-1)}{2}, \dots, 1, 0, 1, \dots, \frac{(N-1)}{2} \right\}$ is first generated by minimizing the predictive cost function based on the discretized current model. This aggregated output level represents the optimal multilevel voltage to be applied by the CHB arm, independently of the specific module-level switching states. Once v_{arm}^* is determined, a dedicated decoding and switching-selection function maps the optimal voltage level to a valid switching configuration of the H-bridge modules. This function handles the redundant switching states (different combinations that generate the same output voltage) and selects the most appropriate one based on simple performance rules. In this work, the redundant-state selection is used to keep the power drawn from each DC source balanced and to spread the switching actions evenly across all devices in 5-level CHB inverter.

E. Unbalanced and Balanced Power-Sharing Switching Methods in a 5-Level CHB inverter

1) *Unbalanced power-sharing switching method:* In the unbalanced power-sharing switching method, the switching table shown in Fig. 5(a) is used. In this scheme, module 1 handles all transitions between the intermediate voltage levels (from 0 to $+v_{\text{DC}}$ or from 0 to $-v_{\text{DC}}$), while module 2

Unbalanced power-sharing			Balanced power-sharing		
$\frac{v_1}{v_{\text{DC}}}$	$\frac{v_2}{v_{\text{DC}}}$	$\frac{v_{\text{arm}}}{v_{\text{DC}}}$	$\frac{v_1}{v_{\text{DC}}}$	$\frac{v_2}{v_{\text{DC}}}$	$\frac{v_{\text{arm}}}{v_{\text{DC}}}$
1	1	2	1	1	2
1	0	1	1	0	1
0	0	0	0	0	0
-1	0	-1	0	-1	-1
-1	-1	-2	-1	-1	-2
(a)			(b)		

Fig. 5. (a) Unbalanced power-sharing (b) balanced power-sharing switching methods in a 5-Level CHB inverter.

switches only when the output reaches the peak levels ($+2v_{\text{DC}}$ or $-2v_{\text{DC}}$). As a result, the switching activity is unevenly distributed, causing higher power dissipation and thermal stress in one module. Additionally, this imbalance is quantitatively expressed in (12), which defines the ratio of the average power delivered by the second H-bridge relative to the total load power for a modulation index $m=1$.

$$\frac{\bar{p}_2}{\bar{p}_1 + \bar{p}_2} = \frac{\frac{1}{\pi} \int_{\pi/6}^{5\pi/6} \hat{v}_{\text{arm}}(\sin(\theta) - 0.5) \cdot i_{\text{arm}} \sin(\theta + \varphi) d\theta}{\frac{1}{2\pi} \int_0^{2\pi} \hat{v}_{\text{arm}} \sin(\theta) \cdot i_{\text{arm}} \sin(\theta + \varphi) d\theta} = 0.391 \quad (12)$$

2) *Balanced power-sharing switching method:* To mitigate uneven power distribution between modules, the balanced power-sharing switching table shown in Fig. 5(b) is employed. In this approach, the gate signals of the two modules are swapped at every half-cycle of the fundamental frequency, ensuring that both modules undergo identical switching activity over time, thereby achieving balanced utilization for $N = 5$. Specifically, balanced power-sharing is realized by alternating module operation in each half-cycle: during the first half-cycle, module 2 is active ($v_{\text{arm}} = v_{\text{DC}}, v_1 = v_{\text{DC}}$ and $v_2 = 0$), and module 1 takes over in the second ($v_{\text{arm}} = -v_{\text{DC}}, v_1 = 0$ and $v_2 = -v_{\text{DC}}$).

IV. SIMULATION RESULTS OF THE PROPOSED MPC WITH BALANCED POWER-SHARING CAPABILITY IN 5-LEVEL CHB INVERTER

Figure. 6 illustrates the performance of the proposed model predictive current controller implemented on a 5-level CHB inverter supplying an RL load ($L = 25$ mH and $R = 40 \Omega$) in PLECS simulations. The nominal DC voltage of each module is $v_{\text{DC},1} = v_{\text{DC},2} = 60$ V. Although the paper investigates both symmetrical and asymmetrical converters, only the 5-level case is presented in the simulations, since the balanced power-sharing method incorporated into the proposed MPC is specifically designed for a 5-level inverter. To investigate the effect of the load inductance on current tracking, simulations were performed for different inductor values of ($L = 10$ mH, 25 mH, and 50 mH), as the predicted currents for all inverter switching states in equation (8) strongly depend on L . The real value is always $L = 25$ mH.

The results highlight a trade-off between current tracking, switching losses, and output voltage distortion.

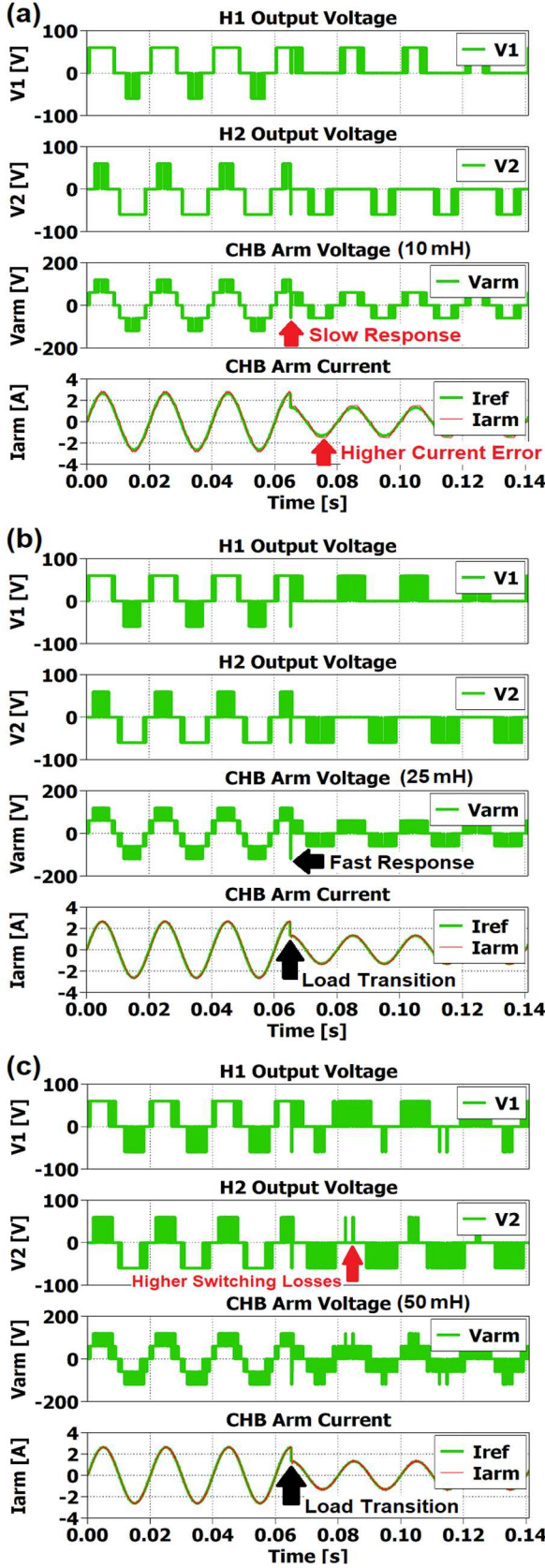


Fig. 6. PLECS-based simulation results of 5-Level CHB inverter under the proposed MPC for different predicted load inductances: (a) 10 mH (underestimation), (b) 25 mH (correct), and (c) 50 mH (overestimation).

1) Figure. 6(a)- $L=10$ mH (underestimated): with a smaller L , the coefficient T_s/L in equation (8) becomes larger, but the term $(1 - RT_s/L)$ reduces faster, causing the real current to respond more slowly to the applied voltage. This slower response increases the deviation from the reference, resulting in higher tracking errors. However, the limited predicted current variations reduce high-frequency switching, keeping switching losses low.

2) Figure. 6(b)- $L = 25$ mH (nominal): here, L matches the actual load, providing a balanced response. The predicted current updates in equation (8) closely match the real dynamics of the RL load, allowing the controller to track the reference accurately without excessive switching.

3) Figure. 6(c)- $L = 50$ mH (overestimated): overestimating L decreases the term T_s/L and increases $(1 - RT_s/L)$, causing the real current to change too aggressively to correct deviations, which increases the number of switching events, resulting in higher switching losses. The aggressive corrections also introduce noticeable distortion in the output voltage waveform, reflecting overcompensation by the controller.

V. EXPERIMENTAL RESULTS

The proposed MPC was implemented on a Typhoon HIL 101 platform and tested on a SiC-MOSFET-based CHB inverter (Fig. 7) supplying an RL load ($L = 25$ mH and $R = 40 \Omega$). The inverter was configured in 5-level ($v_{DC,1} = v_{DC,2} = 60$ V), 7-level ($v_{DC,1} = 80$ V, $v_{DC,2} = 40$ V), 9-level ($v_{DC,1} = 90$ V, $v_{DC,2} = 30$ V) modes to evaluate the controller's performance under different multilevel scenarios. Each configuration enables a varying number of voltage levels at the output, affecting the achievable current ripple and switching frequency.

Figure. 8 presents the experimental results for the 5-level [Fig. 8(a)], 7-level [Fig. 8(b)], and 9-level [Fig. 8(c)] inverters. A step change in the reference load current was applied in each case to assess dynamic performance. The inverter output voltage (blue), load current (green), and reference current (aqua) are shown, with the reference provided by the Typhoon HIL 101, "Analog Out block". In all tested cases, the load current closely follows the reference with minimal overshoot, indicating precise predictive control. Fig. 9 demonstrates the proposed MPC's ability to control power-sharing in a 5-level CHB inverter. In unbalanced mode [Fig. 9(a)], switching pulses concentrate on one module, leading to unequal power-sharing, especially at low current levels where module 2 remains inactive. In balanced mode [Fig. 9(b)], switching pulses are evenly distributed, ensuring equal module utilization across all current levels.

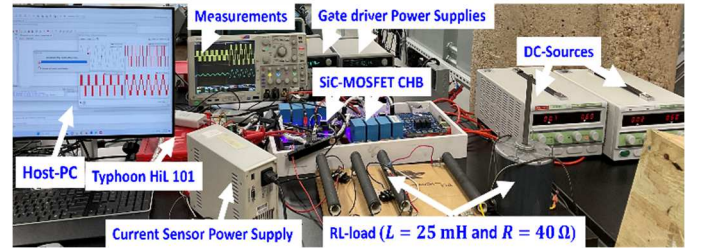


Fig. 7. Experimental setup of a CHB inverter to test the proposed MPC scheme.

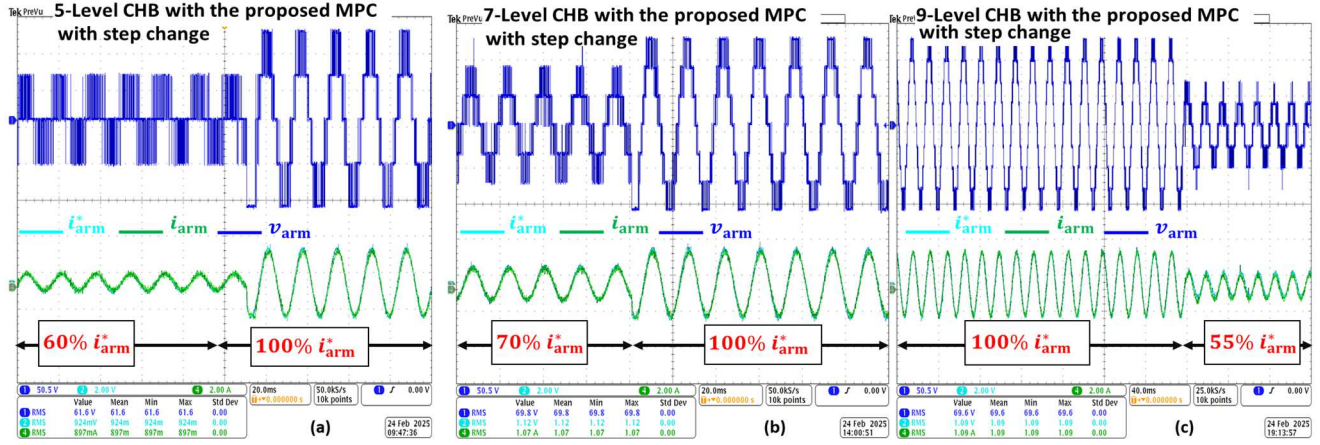


Fig. 8. Test results with the proposed MPC under step changes: (a) 5-level ($v_{DC1} = v_{DC2} = 60V$), (b) 7-Level ($v_{DC1} = 80V, v_{DC2} = 40V$), (c) 9-Level ($v_{DC1} = 90V, v_{DC2} = 30V$).

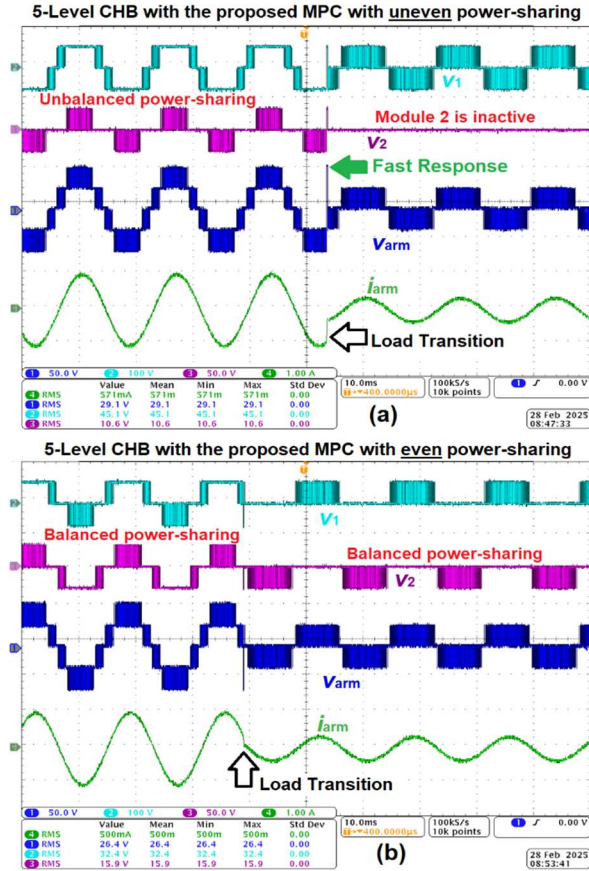


Fig. 9. 5-Level CHB inverter using the proposed MPC with ($v_{DC1} = v_{DC2} = 60V$) in (a) Unbalanced power-sharing and (b) Balanced power-sharing. Current tracking is equally good.

VI. CONCLUSION

This paper presented a generalized model predictive current controller for single-phase CHB inverters, capable of operating with any odd number of voltage levels without increasing control complexity. PLECS-based simulations and experimental results on a SiC-MOSFET prototype operating in 5-, 7-, and 9-level modes demonstrated accurate current tracking, fast dynamic response, and, for the 5-level case, balanced power-

sharing among H-bridge modules. The simulations further highlighted the sensitivity of the MPC to load inductance estimation: underestimating the inductance reduces switching losses with minimal impact on control accuracy, whereas overestimation improves tracking at the expense of higher switching losses and increased output voltage distortion. These results confirm the importance of accurate load modeling for predictive current control. Future work will focus on extending the proposed MPC to achieve effective power balancing in asymmetrical CHB inverter configurations.

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